REMARKS

This paper is responsive to the Non-Final Office Action dated August 5, 2005. Claims 1-25 were examined. Claims 1-7, 11, 15-17 and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,118,316 to Tamamura, et al. in view of U.S. Patent No. 6,353,648 B1 to Suzuki. Claims 10, 12, 13, 18, 19, 22, 23 and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tamamura, in view of Suzuki and U.S. Patent 6,711,227 B1 to Kaylani, et al. Claim 14 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tamamura, et al. in view of Suzuki and U.S. Patent 5,036,298 to Bulzachelli.

Claim Rejections - 35 U.S.C. § 103

Claims 1-7, 11, 15-17 and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,118,316 to Tamamura, et al. in view of U.S. Patent No. 6,353,648 B1 to Suzuki. Regarding claim 1, Applicants respectfully maintain that Tamamura, alone or in combination with Suzuki or other references of record, fails to teach or suggest

> a phase detector circuit coupled to generate a difference signal indicating a phase difference between an incoming data stream and a delayed clock signal; and a clock delay circuit coupled to receive a delay control signal derived from the difference signal and to receive the output clock signal, the clock delay circuit coupled to provide as the delayed clock signal the output clock signal delayed according to the delay control signal,

as required by claim 1. Applicants respectfully maintain that the Office Action fails to establish a *prima facie* case of obviousness.

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of the ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all claim limitations.

See MPEP § 2143. The Office Action relies on divider 204-1 of Tamamura to teach the clock delay circuit of claim 1. Tamamura teaches that divider 204-1 is a frequency divider circuit (col. 15, line 35-col. 18, line 43; Fig. 4). The phase comparator of Tamamura receives a frequency divided signal 204a-1 (Fig. 4), not a delayed clock signal, as required by claim 1. Suzuki fails to compensate for the shortcomings of Tamamura. Suzuki teaches a phase locked loop circuit that feeds back the oscillating output signal of a voltage controlled oscillator and controls the oscillating frequency of the oscillator based on the comparison of the phase between an oscillating output signal and an externally supplied clock signal (col. 2, line 65-col. 3, line 8). Nowhere does Suzuki teach or suggest a phase detector circuit coupled to generate a difference signal indicating a phase difference between an incoming data stream and a delayed clock signal, as required by claim 1.

In addition, the Office Action admits that Tamamura fails to teach or suggest a clock delay circuit receiving a delay control signal derived from the difference signal and to receive an output clock signal, the clock delay circuit coupled to provide as a delayed clock signal the output clock signal delayed according to the delay control signal. The Office Action relies on delay device 7 of Suzuki to supply this teaching. Delay device 7 of Suzuki delays the oscillating output signal to generate timing signal 106, which is supplied to internal circuit 6 (col. 4, lines 20-26). In general, internal circuit 6 of Suzuki is a dynamic circuit that precharges an output during a certain period of a clock and outputs a logic signal during a remaining period of a clock (col. 1, line 10-col. 2, line 53). Delaying an oscillating output signal to control a dynamic circuit fails to teach or suggest a phase detector circuit coupled to generate a difference signal indicating a phase difference between an incoming data stream and the delayed clock signal, the delayed clock signal being provided based on a delay control signal derived from the difference signal as required by claim 1.

Applicants respectfully maintain that the Office Action fails to provide a teaching or suggestion to combine, and Applicants respectfully maintain that there is no teaching or suggestion to combine, delay device 7 and timing signal 106 of Suzuki with frequency divider circuit 204 of a PLL of Fig. 4 of Tamamura, to provide the combination of claim 1. For at least these reasons, Applicants believe that claim 1 is allowable over the art of record. Accordingly,

Applicants respectfully request that the rejection of claim 1 and all claims dependent thereon, be withdrawn.

Regarding claim 15, Applicants respectfully maintain that Tamamura, alone or in combination with Suzuki or other references of record fails to teach or suggest

> determining a phase difference between an input data stream and a delayed clock signal and generating a difference signal indicative thereof; and receiving the output clock signal in a delay circuit and generating the delayed clock signal from the output clock signal according to a delay control signal derived from the difference signal,

as required by claim 15. Applicants respectfully maintain that the Office Action fails to establish a *prima facie* case of obviousness. See MPEP § 2143. The Office Action relies on divider 204-1 of Tamamura to provide a delayed clock signal of claim 15. Tamamura teaches that divider 204-1 is a frequency divider circuit (col. 15, line 35-col. 18, line 43; Fig. 4). The phase comparator of Tamamura receives a frequency divided signal 204a-1 (Fig. 4), not a delayed clock signal, as required by claim 15. Suzuki fails to compensate for the shortcomings of Tamamura. Suzuki teaches a phase locked loop circuit that feeds back the oscillating output signal of a voltage controlled oscillator and controls the oscillating frequency of the oscillator based on the comparison of the phase between an oscillating output signal and an externally supplied clock signal (col. 2, line 65-col. 3, line 8). Nowhere does Suzuki teach or suggest determining a phase difference between an input data stream and a delayed clock signal and generating a difference signal indicative thereof, as required by claim 15.

In addition, the Office Action admits that Tamamura fails to teach or suggest a clock delay circuit receiving a delay control signal derived from the difference signal and to receive an output clock signal, the clock delay circuit coupled to provide as a delayed clock signal the output clock signal delayed according to the delay control signal. The Office Action relies on delay device 7 of Suzuki to supply this teaching. Delay device 7 of Suzuki delays the oscillating output signal to generate timing signal 106, which is supplied to internal circuit 6 (col. 4, lines

20-26). In general, internal circuit 6 of Suzuki is a dynamic circuit that precharges an output during a certain period of a clock and outputs a logic signal during a remaining period of a clock (col. 1, line 10-col. 2, line 53). Delaying an oscillating output signal to control a dynamic circuit fails to teach or suggest determining a phase difference between an input data stream and a delayed clock signal and generating a difference signal indicative thereof and receiving the output clock signal in a delay circuit and generating the delayed clock signal from the output clock signal according to a delay control signal derived from the difference signal, as required by claim 15.

Applicants respectfully maintain that the Office Action fails to provide a teaching or suggestion to combine, and Applicants respectfully maintain that there is no teaching or suggestion to combine, delay device 7 and timing signal 106 of Suzuki with frequency divider circuit 204 of a PLL of Fig. 4 of Tamamura, to provide the combination of claim 15. For at least these reasons, Applicants believe that claim 15 is allowable over the art of record. Accordingly, Applicants respectfully request that the rejection of claim 15 and all claims dependent thereon, be withdrawn.

Claim 24 is amended to correct a typographical error. Regarding claim 24, Applicants respectfully maintain that Tamamura, alone or in combination with Suzuki or other references of record fails to teach or suggest

> means for detecting a phase difference between an incoming data stream and a delayed clock signal and generating a difference signal indicative thereof; and
> means for generating the delayed clock signal from the clock signal according to a delay control signal derived from the difference signal,

as required by claim 24. Applicants respectfully maintain that the Office Action fails to establish a *prima facie* case of obviousness. See MPEP § 2143. The Office Action relies on divider 204-1 of Tamamura to provide a delayed clock signal of claim 24. Tamamura teaches that divider 204-1 is a frequency divider circuit (col. 15, line 35-col. 18, line 43; Fig. 4). The phase comparator of Tamamura receives a frequency divided signal 204a-1 (Fig. 4), not a delayed clock signal, as

required by claim 24. Suzuki fails to compensate for the shortcomings of Tamamura. Suzuki teaches a phase locked loop circuit that feeds back the oscillating output signal of a voltage controlled oscillator and controls the oscillating frequency of the oscillator based on the comparison of the phase between an oscillating output signal and an externally supplied clock signal (col. 2, line 65-col. 3, line 8). Nowhere does Suzuki teach or suggest detecting a phase difference between an incoming data stream and a delayed clock signal and generating a difference signal indicative thereof, as required by claim 24.

In addition, the Office Action admits that Tamamura fails to teach or suggest a clock delay circuit receiving a delay control signal derived from the difference signal and to receive an output clock signal, the clock delay circuit coupled to provide as a delayed clock signal the output clock signal delayed according to the delay control signal. The Office Action relies on delay device 7 of Suzuki to supply this teaching. Delay device 7 of Suzuki delays the oscillating output signal to generate timing signal 106, which is supplied to internal circuit 6 (col. 4, lines 20-26). In general, internal circuit 6 of Suzuki is a dynamic circuit that precharges an output during a certain period of a clock and outputs a logic signal during a remaining period of a clock (col. 1, line 10-col. 2, line 53). Delaying an oscillating output signal to control a dynamic circuit fails to teach or suggest detecting a phase difference between an incoming data stream and a delayed clock signal and generating a difference signal indicative thereof and means for generating the delayed clock signal from the clock signal according to a delay control signal derived from the difference signal, as required by claim 24.

Applicants respectfully maintain that the Office Action fails to provide a teaching or suggestion to combine, and Applicants respectfully maintain that there is no teaching or suggestion to combine, delay device 7 and timing signal 106 of Suzuki with frequency divider circuit 204 of a PLL of Fig. 4 of Tamamura, to provide the combination of claim 24. For at least these reasons, Applicants believe that claim 24 is allowable over the art of record. Accordingly, Applicants respectfully request that the rejection of claim 24 and all claims dependent thereon, be withdrawn.

Claims 10, 12, 13, 18, 19, 22, 23 and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tamamura, in view of Suzuki and U.S. Patent 6,711,227 B1 to Kaylani, et al.

Applicants respectfully maintain that claims 10, 12, 13, 18, 19, 22, 23, and 25 depend from allowable base claims and are allowable for at least this reason. Accordingly, Applicants respectfully request that the rejection of these claims be withdrawn.

Claim 14 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tamamura, et al. in view of Suzuki and U.S. Patent 5,036,298 to Bulzachelli. Applicants respectfully maintain that Tamamura and Suzuki, alone or in combination with Bulzachelli or other references of record, fails to teach or suggest

a closed loop response without an explicit zero,

as recited by claim 14. The Office Action relies on Tamamura and Suzuki in combination with Bulzachelli to supply this teaching. As described above, Tamamura and Suzuki fail to teach or suggest the limitations of claim 1. Assuming arguendo that Tamamura and Suzuki teach the limitations of claim 1, the Office Action fails to provide a *prima facie* case of obviousness for claim 14. The Office Action admits that Tamamura fails to teach a closed loop response without an explicit zero and relies on Bulzachelli to supply this teaching. However, the Office Action fails to provide a motivation to combine the teachings of Tamamura and Suzuki to have the closed loop response of Bulzachelli and Applicants respectfully maintain that there is no motivation to combine the teachings of Tamamura and Suzuki to have the closed loop response of Bulzachelli. "[S]imply identifying all of the elements in a claim in the prior art does not render a claim obvious. Ruiz, 357 F.3d at 1275. Instead section 103 requires some suggestion or motivation in the prior art to make the new combination. Rouffet, 149 F.3d at 1355-56." Princeton Biochemicals, Inc. v. Beckman Coulter, Inc., No. 04-1493, slip op. at 10 (Fed. Cir., June 9, 2005). Thus, Tamamura and Suzuki, alone or in combination with other references of record, fail to teach or suggest the clock recovery circuit of claim 1 with a closed loop response without an explicit zero. For at least this reason, Applicants respectfully maintain that claim 14 distinguishes over Tamamura and Suzuki, alone or in combination with all references of record. Accordingly, Applicants respectfully request that the rejection of claim 14 be withdrawn.

Allowable Subject Matter

Claims 8, 9, 20 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants appreciate the indication of allowable subject matter in claims 8, 9, 20, and 21. Applicants respectfully maintain that claims 8, 9, 20 and 21 depend from allowable base claims and are allowable for at least this reason. Accordingly, Applicants respectfully request that the objections to these claims be withdrawn.

Summary

Claims 1-25 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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